Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A digital-to-analog converting circuit comprising:

a first potential terminal for supplying a first potential;

a second potential terminal for supplying a second potential;

an output node for outputting an analog signal;

a first ~~resister~~ resistor circuit having a plurality of first ~~resisters~~ resistors connected in series between a first node and the output node through a plurality of first connecting points;

a first switching circuit having a plurality of first switches each of which is connected between the first potential terminal and one of the first connecting points and the first node;

a second ~~resister~~ resistor circuit having a plurality of second ~~resisters~~ resistors connected in series between a second node and the output node through a plurality of second connecting points;

a second switching circuit having a plurality of second switches each of which is connected between the second potential terminal and one of the second connecting points and the second node; and

a control circuit connected to the first and second switching circuits for controlling the first and second switches.

Claim 2 (Original): A digital-to-analog converting circuit according to claim 1, wherein the first switching circuit further has a first switch connected between the first potential terminal and the output node.

Claim 3 (Original): A digital-to-analog converting circuit according to claim 1, wherein the second switching circuit further has a second switch connected between the second potential terminal and the output node.

Claim 4 (Original): A digital-to-analog converting circuit according to claim 1, wherein the first switches are P-channel type MOS transistors and the second switches are N-channel type MOS transistors.

Claim 5 (Original): A digital-to-analog converting circuit according to claim 1, wherein the control circuit includes a first decoder for controlling the first switches and a second decoder for controlling the second switches.

Claim 6 (Original): A digital-to-analog converting circuit according to claim 1, wherein the first potential is a reference potential and the second potential is a ground potential.

Claim 7 (Original): A digital-to-analog converting circuit according to claim 1, further comprising an amplifier connected to the output node for amplifying the analog signal.

Claim 8 (Currently Amended): A digital-to-analog converting circuit comprising:

a first potential terminal supplying a first potential;

a second potential terminal supplying a second potential;

an output node providing an analog signal;

a plurality of first ~~resisters~~ resistors connected in series between a first node and the output node, the first ~~resisters~~ resistors being connected to each other at a plurality of first connecting points;

a plurality of first switches each of which is connected between the first potential terminal and one of the first connecting points and the first node;

a plurality of second ~~resisters~~ resistors connected in series between a second node and the output node, the second ~~resisters~~ resistors being connected to each other at a plurality of second connecting points;

a plurality of second switches each of which is connected between the second potential terminal and one of the second connecting points and the second node; and

a control circuit connected to control the first and second switches.

Claim 9 (Original): A digital-to-analog converting circuit according to claim 8 , further comprising an additional first switch connected between the first potential terminal and

the output node.

Claim 10 (Original): A digital-to-analog converting circuit according to claim 8, further comprising an additional second switch connected between the second potential terminal and the output node.

Claim 11 (Original): A digital-to-analog converting circuit according to claim 8, wherein the first switches are P-channel type MOS transistors and the second switches are N-channel type MOS transistors.

Claim 12 (Original): A digital-to-analog converting circuit according to claim 8, wherein the control circuit includes a first decoder for controlling the first switches and a second decoder for controlling the second switches.

Claim 13 (Original): A digital-to-analog converting circuit according to claim 8, wherein the first potential is a reference potential and the second potential is a ground potential.

Claim 14 (Original): A digital-to-analog converting circuit according to claim 8, further comprising an amplifier connected to the output node for amplifying the analog signal.

Claim 15 (Currently Amended): A digital-to-analog converting circuit comprising:

a first potential terminal supplying a first potential;

a second potential terminal supplying a second potential;

an analog node providing an analog signal;

a plurality of first ~~resisters~~ resistors connected in series between a first node and the analog node through a plurality of first connecting nodes;

a plurality of first switches each of which is connected between the first potential terminal and one of the first connecting nodes and the first node;

a plurality of second ~~resisters~~ resistors connected in series between a second node and the output node through a plurality of second connecting nodes;

a plurality of second switches each of which is connected between the second potential terminal and one of the second connecting nodes and the second node; and

a control circuit connected to control the first and second switches.

Claim 16 (Original): A digital-to-analog converting circuit according to claim 15, further comprising an additional first switch connected between the first potential terminal and the output node.

Claim 17 (Original): A digital-to-analog converting circuit according to claim 15, further comprising an additional second switch connected between the second potential terminal and the output node.

Claim 18 (Original): A digital-to-analog converting circuit according to claim 15, wherein the first switches are P-channel type MOS transistors and the second switches are N-channel type MOS transistors.

Claim 19 (Original): A digital-to-analog converting circuit according to claim 15, wherein the control circuit includes a first decoder for controlling the first switches and a second decoder for controlling the second switches.

Claim 20 (Original): A digital-to-analog converting circuit according to claim 15, wherein the first potential is a reference potential and the second potential is a ground potential.

Claim 21 (Original): A digital-to-analog converting circuit according to claim 15, further comprising an amplifier connected to the output node for amplifying the analog signal.